CDA-5106 Assignment 2

3.15

3.16

1. LD F1 X
2. LD F2 Y
3. ADD F4 F1 Z
4. MUL F3 F1 F2
5. LD F2 Z
6. MUL F3 F3 F2
7. ADD F4 F5 F6
8. ADD F4 F1 F2

Since the MUL instructions take 15 cycles, and the second instruction (Line 6) is dependent on the first one (Line 4), it will begin execution at the 22nd clock cycle. In the meantime, the ADD instructions can begin execution since there is no data dependence between them and the MUL instructions. However, each of the ADD instructions is dependent on each other so they cannot execute concurrently.

We assume that Load operations take 2 cycles. We also assume that X, Y and Z are already present in the registers.

There will be CDB contention in the 38th cycle when instructions 6 and 8 complete their execution at the same time.

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| Instruction number | Issue cycle | Starting cycle | Finishing cycle | Write back cycle |
| 1 | 1 | 2 | 4 | 5 |
| 2 | 2 | 3 | 5 | 6 |
| 3 | 3 | 5 | 15 | 16 |
| 4 | 4 | 6 | 21 | 22 |
| 5 | 5 | 7 | 9 | 10 |
| 6 | 6 | 22 | 37 | 38 |
| 7 | 7 | 16 | 26 | 27 |
| 8 | 8 | 27 | 37 | 38 |

3.17

3.18